

DAQ, Controls and Engineering

30 April 2014

Topics

DAQ

- the RSI & ESE departments work on development of large scale DAQ systems for experiments
- current experiments include NOvA, Mu2e, LBNE, MicroBooNE, Darkside-50, test beams
- focus is on "back-end" DAQ electronics and software

Controls

- detector timing systems
- detector control systems (DCS) ("slow controls")

Engineering

- DAQ hardware for experiments (Mu2e, NOvA) and test beams (CAPTAN)
- generic R&D in areas such as optical links (CMS) and CCDs/MKIDs (astronomy)
- accelerator instrumentation and "front-end" electronics to support AD & PPD projects

definitions

- "back-end DAQ" - the electronics and software used to transmit and process data
- "front-end DAQ" - the electronics used to digitize data

Issues

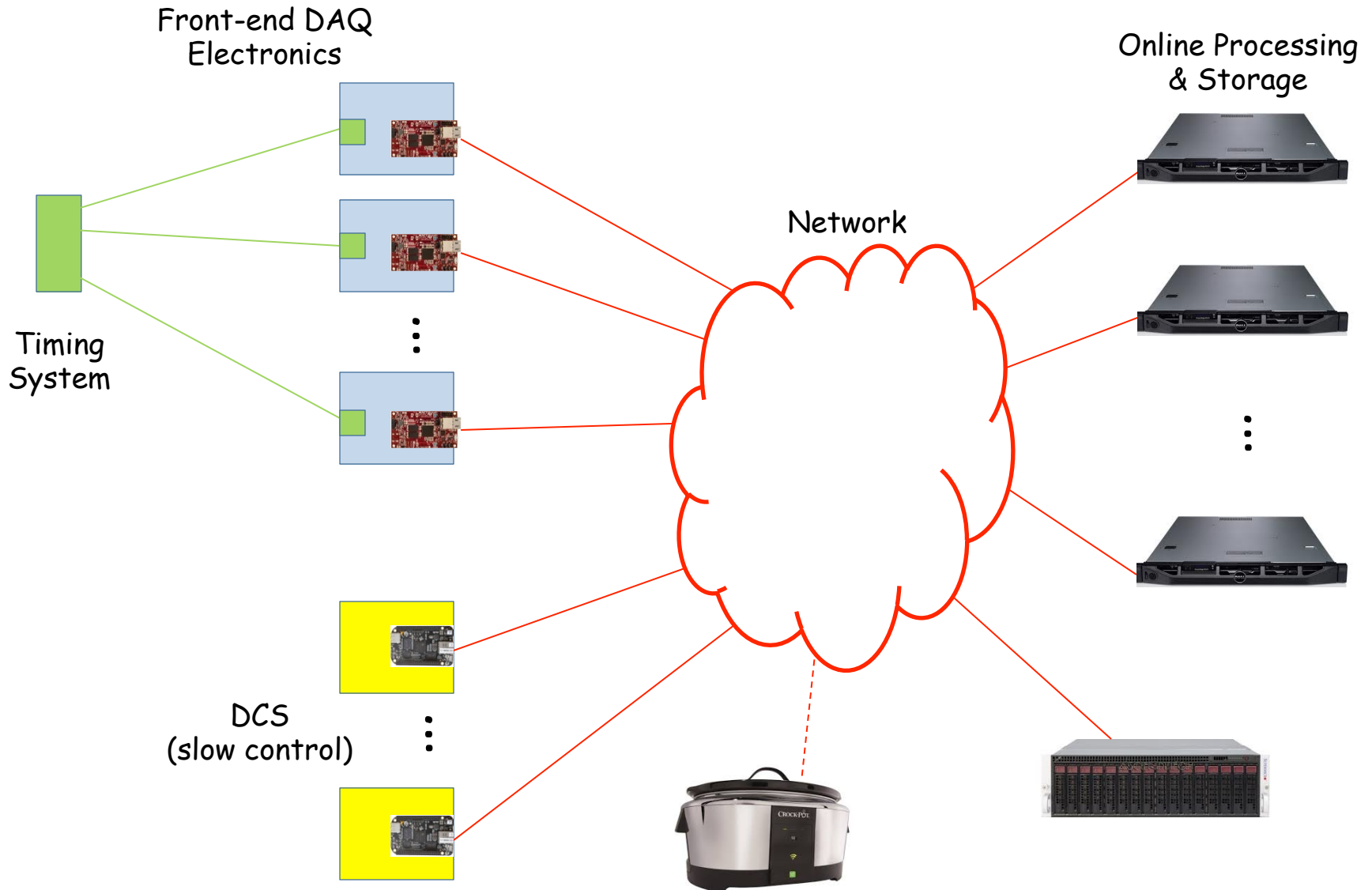
- experiments are looking for off-the-shelf DAQ solutions with minimal R&D cost
- can't rely on projects as primary funding source for future DAQ R&D
- large scale DAQ systems can now be implemented using little or no custom back-end hardware
- difficult to support partnerships with experiments AND development new systems at current resource levels
- current DCS ("slow controls") and DAQ systems are based on dissimilar hardware and software

Proposals

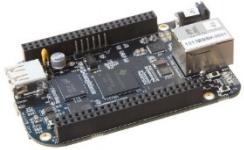
- develop scalable off-the-shelf DAQ system, based on full-featured artdaq and “Internet of Things” (IoT) architecture
- concentrate on intelligent front-ends
- use commercial & open source hardware for back-end DAQ
- general shift toward more software & firmware vs hardware design work
- ESE should improve capability in embedded software (additional training)
- expand effort in online processing applications using GPUs, many-core processors, FPGAs
- continue development work on MKIDs and CMS optical links (diversity)
- focus on expertise in firmware, real-time software for CMS upgrade work
- integrate Detector Control, Timing, and DAQ as part of off-the-shelf system

Supplemental Slides

IoT DAQ



IoT DAQ



2,500 DMIPS CPU
100M Ethernet
\$50



10,000 DMIPS CPU*
1G Ethernet
\$130



4,000 DMIPS CPU
+ 20,000 DMIPS FPGA
1G Ethernet
\$200



48 port 1G
4 GBytes/sec
\$1,300

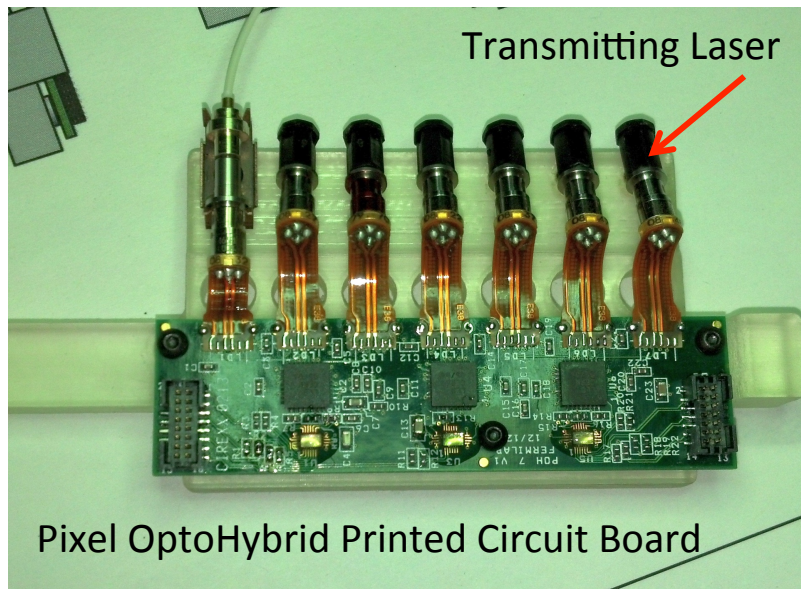


48 port 10G
40 GBytes/sec**
\$13,000

* equivalent to 50 Cray-1 supercomputers
** equivalent to 1,000 VME backplanes

- Low-cost commercial boards (running LINUX and embedded artdaq) can be used to connect front-end electronics directly to a network.
- Network bandwidth is almost free (< \$500 per GByte/sec).

ESE Optical Links R&D

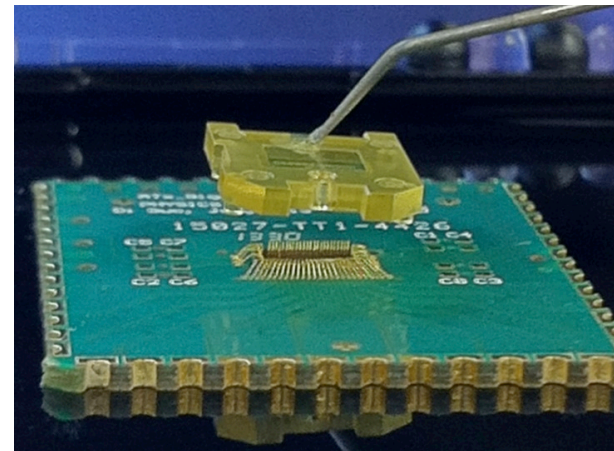


CMS Phase 1 FPix Upgrades

ESE to deliver 120 Pixel OptoHybrids for Phase 1 Upgrades

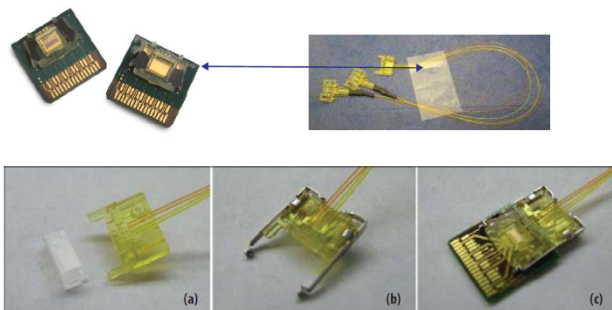
In addition to the POH devices, we are instrumenting a full readout chain test bench.

DOE Optical Links R&D



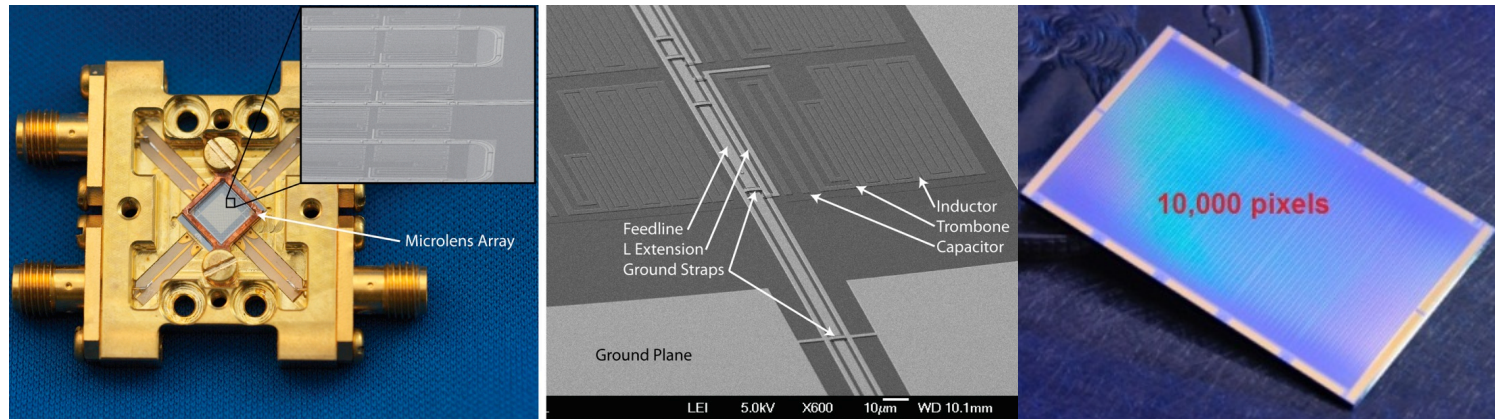
Provide system testing support for 120 Gbps (10 Gbps x 12 channels) custom transmitter (rad hard, low mass)

Versatile Link Plus



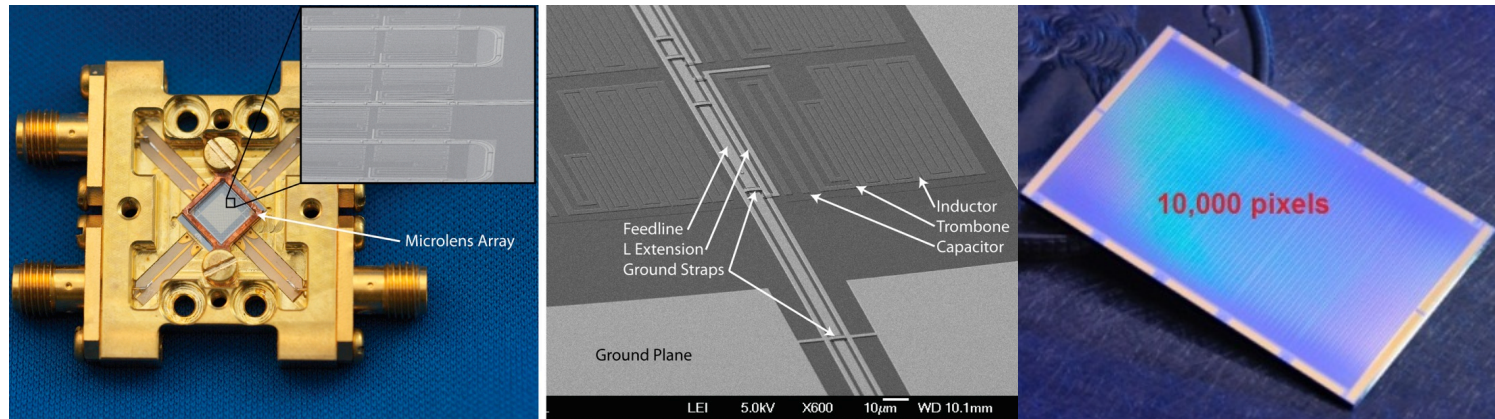
Goal: Engineer 10 Gbps optical links in flexible formats for CMS Phase II

MKIDs (Microwave Kinetic Inductance Devices)



- R&D and candidate instruments based on MKIDs at FNAL: Spectroscopy of DES and LSST images, large instrument for CMB (generation 4)
- Size of the instrument seriously constrained by cost and size of the DAQ... need to reduce cost from \$50/pixel to < \$5/pixel.
- Input bandwidth: ~ 0.5 TB/s for 10K pixels
- Output bandwidth: ~ 100 MB/s for 10K pixels

MKIDs (Microwave Kinetic Inductance Devices)



- R&D and candidate instruments based on MKIDs at FNAL: 20K pixel instrument for SOAR. Spectroscopy of DES and LSST images, large instrument for CMB (generation 4)
- Size of the instrument seriously constrained by cost and size of the DAQ. The ESE DAQ will reduce cost from \$50/pixel to < \$5/pixel.
- Input bandwidth: ~ 0.5 TB/s for 10K pixels
- Output bandwidth: ~ 100 MB/s for 10K pixels